FORM PTO-1449 LIST OF DOCUMENTS CITED BY APPLICANT	Atty. Docket No. XA-9485A	Appln. No.
	Applicant Masaya MURANAKA et al.	
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Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
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TB	AP	Mano, T.; Yamada, J.; Inoue, J.; Nakajima, S.; Circuit Techniques For A VLSI Memory, IEEE Journal of Solid-State Circuits, Volume: 18 Issue: 5, October 1983, Pages 463-470
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Examiner	/Timothy Bonura/	Date Considered	10/05/2006

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.